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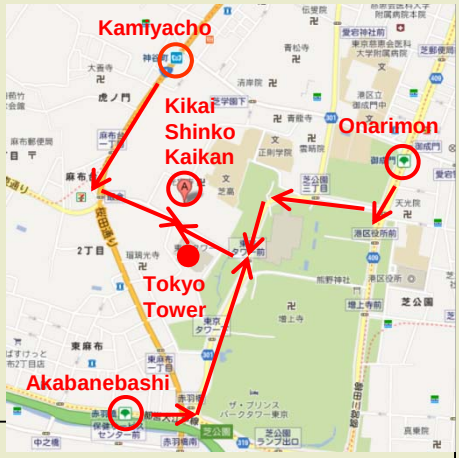
2nd JST International Symposium on Dependable VLSI Systems (DVLSI 2013)

December 6-7, 2013

Kikai Shinko Kaikan Building, Tokyo, Japan

Sponsored by JST CREST/DVLSI
Co-Sponsored by Kyushu Institute of Technology
In cooperation with the IEICE Electronics Society Technical Committee on Integrated Circuits and Devices (tentative)
In cooperation with the IEICE Information and Systems Society Technical Committee on Dependable Computing

This is an announcement of the second JST International Symposium of Dependable VLSI Systems to be held in Tokyo on December 6-7, 2013. The purpose of this meeting is to review and discuss the progress and outcome of a research program entitled, "Dependable VLSI Systems (DVLSI)" among professionals having special interest in the dependability of electronic systems. This unique program, sponsored by JST (Japan Science and Technology Agency), was initiated in 2007 for the purpose of developing basic VLSI technologies to enhance the dependability of systems. The program addresses various important issues of dependability ranging from the chip level all the way up to the systems level. Systems addressed include automotive, robotic, plant control, transportation, telecom, data processing to aerospace. The program consists of eleven (11) projects which has dealt with key issues, some arising from small feature sizes and others from design complexity. At the symposium this year, all eleven projects are reviewed including those which completed the term of five years and a half in March 2013. We will solicit guest speakers and panelists from various organizations of excellence where related objectives are being pursued. Invitation is being extended to everybody who has ever attended the past DVLSI meetings or to anybody who has special interest in the systems dependability and its implications in VLSI.



Venue
Kikai Shinko Kaikan Building,
3-5-8 Shibakoen, Minato-ku, Tokyo 105-0011 Japan
Access
1. 6-minute walk from Kamiyacho Sta., Tokyo Metro Hibiya Line
2. 8-minute walk from Onarimon Sta., Toei Mita Line
3. 10-minute walk from Akabanebashi Sta., Toei Oedo Line
http://www.jspmi.or.jp/kaigishitsu/access.html

Registration
Invited attendees: Invitation will be extended to solicit attendance.
General registration: welcome to pre-register at http://www.dvlsi.jst.go.jp/english/index.html
Registration Fee: free for all sessions, and 6000 JPY for banquet
Contact: symposium secretariat (k2tsujim@jst.go.jp or dvlsi@dvlsi.jst.go.jp)

DVLSI

JST/CREST Program 'Dependable VLSI Systems'
http://www.dvlsi.jst.go.jp/english/index.html"

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Koichiro Takayama	(Chief Researcher, Fujitsu Laboratory Ltd.)

Principal Investigators and Research Themes

1. Hidetoshi Onodera (Kyoto University) URL http://www.tamaru.kuee.kyoto-u.ac.jp/
   "Dependable VLSI platform using robust fabrics"
2. Shuichi Sakai (The University of Tokyo) URL http://www.mtl.t.u-tokyo.ac.jp/index-e.html
   "Ultra Depedable VLSI by collaboration of formal verifications and architectural technologies"
3. Kazuo Tsubouchi (Tohoku University) URL http://www.riec.tohoku.ac.jp/lab/it-21-mob/index-e.html
   "Development of Dependable Wireless System and Device"
4. Hiroto Yasuura (Kyushu University) URL http://soc.ait.kyushu-u.ac.jp/SOC/
   "Modeling, Detection, Correction and Recovery Techniques for Unified Dependable Design"
5. Seiji Kajihara (The Kyushu Institute of Technology) URL http://aries3a.cse.kyutech.ac.jp/
   "Circuit and system mechanisms for high field reliability"
6. Masahiko Yoshimoto (Kobe University) URL http://www28.cs.kobe-u.ac.jp/en/
   "Dependable SRAM Techniques for Highly Reliable VLSI System"
7. Tomohiro Yoneda (National Institute of Informatics) URL http://www.nii.ac.jp/staff/Yoneda_Tomohiro.shtml
   "Development of Dependable Network-on-Chip Platform"
8. Mitsumasa Koyanagi (Tohoku University) URL http://www.sd.mech.tohoku.ac.jp/Site/Home.html
   "Three-Dimensional VLSI System with Self-Restoration Function"
9. Ken Takeuchi (Chuo University) URL http://www.takeuchi-lab.org/index_e.htm
   "Dependable Wireless Solid-State Drive (SSD)"
10. Takeshi Fujino (Ritsumeikan University) URL http://www.ritsumei.ac.jp/se/re/fujinolab/index-e.html
    "The Design and Evaluation Methodology of Dependable VLSI for Tamper Resistance"
11. Nobuyuki Yamasaki (Keio University) URL http://www.ny.ics.keio.ac.jp/
    "Fundamental Technology on Dependable SoC and SiP for Embedded Real-Time Systems"

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